

# Notice of Allowability

Application No.

09/922,763

Examiner

Negussie Worku

Applicant(s)

TAKADA ET AL.

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## -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 08/06/01.
2. ☒ The allowed claim(s) is/are 1-41.
3. ☒ The drawings filed on 06 August 2001 are accepted by the Examiner.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) ☒ All    b) ☐ Some\*    c) ☐ None    of the:
    1. ☒ Certified copies of the priority documents have been received.
    2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

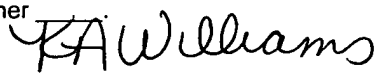
Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.  
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
  6. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
    - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.
    - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

### Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08),  
Paper No./Mail Date 08/06/01
4. ☐ Examiner's Comment Regarding Requirement for Deposit  
of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413),  
Paper No./Mail Date \_\_\_\_\_.
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other



  
**KIMBERLY WILLIAMS**  
**SUPERVISORY PATENT EXAMINER**

## **DETAILED ACTION**

### ***Reasons for Allowance***

1. The following is an examiner's statement of reasons for allowance: With respect to claim 1, the prior art does not teach or disclose a solid-state image-sensing device comprising: a light-sensing element that produces an electric signal commensurate with an amount of light incident thereon; a transistor of which a first electrode and a control electrode are connected to one electrode of the light-sensing element; and a resetting portion for resetting the transistor by feeding a predetermined pulse signal to a second electrode of the transistor, wherein the resetting portion resets the transistor in such a way as to inhibit the transistor from operating in a sub-threshold region when the amount of light incident on the light-sensing element is below a predetermined level.

With respect to claim 2, the prior art does not teach or disclose a solid-state image-sensing device comprising: a light-sensing element that produces an electric signal commensurate with an amount of light incident thereon; a transistor of which a first electrode and a control electrode are connected to one electrode of the light sensing element; and a resetting portion for resetting the transistor by feeding a

predetermined pulse signal to a second electrode of the transistor, wherein the resetting portion resets the transistor in such a way as to permit the transistor to operate in a sub threshold region when the amount of light incident on the light-sensing element is equal to or above a predetermined level.

With respect to claim 3, the prior art does not teach or disclose a solid-state image-sensing device comprising: a light-sensing element that produces an electric signal commensurate with an amount of light incident thereon; a transistor of which a first electrode and a control electrode are connected to one electrode of the light-sensing element; and a resetting portion for resetting the transistor by feeding a predetermined pulse signal to a second electrode of the transistor, wherein the resetting portion resets the transistor in such a way as to keep the transistor in a cut-off state when the amount of light incident on the light-sensing element is below a predetermined level and permit the transistor to operate in a sub-threshold region when the amount of light incident on the light-sensing element is equal to or above the predetermined level.

With respect to claim 4, the prior art does not teach or disclose a solid-state image-sensing device comprising: a light-sensing element that produces an electric signal commensurate with an amount of light incident thereon; a transistor of which a first electrode and a control electrode are connected to one electrode of the light-sensing element; and a resetting portion for resetting the transistor by feeding a predetermined pulse signal to a second electrode of the transistor, wherein the resetting

portion resets the transistor in such a way as to keep the transistor in a cut-off state when the amount of light incident on the light-sensing element is below a predetermined level so that an output linearly proportional to the amount of light incident on the light-sensing element appears at the control electrode of the transistor and permit the transistor to operate in a sub-threshold region when the amount of light incident on the light-sensing element is equal to or above the predetermined level so that an output logarithmically proportional to the amount of light incident on the light-sensing element appears at the control electrode of the transistor.

With respect to claims 5-11, the prior art does not teach or disclose a solid-state image-sensing device having a plurality of pixels each comprising a light-sensing element that produces an electric signal commensurate with an amount of light incident thereon, wherein each pixel further comprises a transistor of which a first electrode and a control electrode are connected to one electrode of the light-sensing element, the solid-state image-sensing device further has a resetting portion for resetting the transistor by feeding a predetermined pulse signal to a second electrode of the transistor, and the resetting portion resets the transistor in such a way as to keep the transistor in a cut-off state when the amount of light incident on the light-sensing element is below a predetermined level so that an output linearly proportional to the amount of light incident on the light-sensing element appears at the control electrode of the transistor and permit the transistor to operate in a sub-threshold region when the amount of light incident on the light-sensing element is equal to or above the

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predetermined level so that an output logarithmically proportional to the amount of light incident on the light-sensing element appears at the control electrode of the transistor.

With respect to claim 12, the prior art does not teach or disclose a solid-state image-sensing device comprising: a light-sensing element that produces an electric signal commensurate with an amount of light incident thereon; a transistor of which a second electrode is connected to one electrode of the light-sensing element; and a resetting portion for resetting the transistor, wherein the resetting portion resets the transistor by feeding a predetermined second pulse signal to a control electrode of the transistor and a predetermined first pulse signal to a first electrode of the transistor in such a way as to keep the transistor in a cut-off state when the amount of light incident on the light-sensing element is below a predetermined level and permit the transistor to operate in a sub threshold region when the amount of light incident on the light-sensing element is equal to or above the predetermined level.

With respect to claim 13, the prior art does not teach or disclose a solid-state image-sensing device comprising: a light-sensing element that produces an electric signal commensurate with an amount of light incident thereon; a transistor of which a second electrode is connected to one electrode of the light-sensing element; and a resetting portion for resetting the transistor, wherein the resetting portion resets the transistor by feeding a predetermined pulse voltage, in a range in which a potential at

the second electrode of the transistor reflects a threshold level of the transistor, to at least the control electrode of the transistor in such a way as to keep the transistor in a cut-off state when the amount of light incident on the light-sensing element is below a predetermined level and permit the transistor to operate in a sub-threshold region when the amount of light incident on the light-sensing element is equal to or above the predetermined level.

With respect to claims 14-17, the prior art does not teach or disclose a solid-state image-sensing device having a plurality of pixels each comprising a light-sensing element that produces an electric signal commensurate with an amount of light incident thereon, wherein each pixel further comprises a transistor of which a second electrode is connected to one electrode of the light-sensing element and that receives a first pulse signal having a first voltage at a first electrode thereof and a second pulse signal having a second voltage at a control electrode thereof during resetting, a voltage at the second electrode of the transistor is reset through the transistor as a result of the first pulse signal being fed to the first electrode of the transistor and the second pulse signal being fed to the control electrode of the transistor, and the transistor is kept in a cut-off state when the amount of light incident on the light-sensing element is below a predetermined level so that an output linearly proportional to the amount of light incident on the light-sensing element appears at the second electrode of the transistor and made to operate in a sub-threshold region when the amount of light incident on the light-sensing element is equal to or above the predetermined level so that an output logarithmically

proportional to the amount of light incident on the light-sensing element appears at the second electrode of the transistor.

With respect to claims 18-32, the prior art does not teach or disclose a solid-state image-sensing device having a plurality of pixels, wherein each pixel comprises: a photodiode that receives a direct-current voltage at a first electrode thereof, and a first MOS transistor of which a first electrode and a gate electrode are connected to a second electrode of the photodiode and that receives a pulse signal having a predetermined voltage at a second electrode thereof, a voltage at the gate electrode of the first MOS transistor is reset through the first MOS transistor as a result of the pulse signal being fed to the second electrode of the first MOS transistor, and the first MOS transistor is kept in a cut-off state when an amount of light incident on the photodiode is below a predetermined level so that an output linearly proportional to the amount of light incident on the photodiode appears at the gate electrode of the first MOS transistor and made to operate in a sub-threshold region when the amount of light incident on the photodiode is equal to or above the predetermined level so that an output logarithmically proportional to the amount of light incident on the photodiode appears at the gate electrode of the first MOS transistor.

With respect to claims 33-41, the prior art does not teach or disclose a solid-state image-sensing device having a plurality of pixels, wherein each pixel comprises: a photodiode that receives a direct-current voltage at a second electrode thereof, and a

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first MOS transistor of which a second electrode is connected to a first electrode of the photo diode and that receives a first pulse signal having a first voltage at a first electrode thereof and a second pulse signal having a second voltage at a gate electrode thereof, a voltage at the second electrode of the first MOS transistor is reset through the first MOS transistor as a result of the first pulse signal being fed to the first electrode of the first MOS transistor and then the second pulse signal being fed to the gate electrode of the first MOS transistor, and the first MOS transistor is kept in a cut-off state when an amount of light incident on the photodiode is below a predetermined level so that an output linearly proportional to the amount of light incident on the photodiode appears at the second electrode of the first MOS transistor and made to operate in a sub-threshold region when the amount of light incident on the photodiode is equal to or above the predetermined level so that an output logarithmically proportional to the amount of light incident on the photodiode appears at the second electrode of the first MOS transistor.


2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Negussie Worku whose telephone number is 305-5441. The examiner can normally be reached on 7am-4pm.

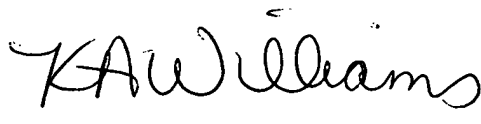
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly Williams can be reached on 703-305-4863. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.



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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Negussie Warku  
03/03/05

  
**KIMBERLY WILLIAMS**  
**SUPERVISORY PATENT EXAMINER**